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**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED  
UNAVOIDABLY UNDER 37 CFR 1.137(a)**

Docket Number (Optional)  
14701

First Named Inventor: SYUUICHI KARIYAZAKI

Art Unit: 2811

Application Number: 09/876,396

Examiner: Douglas W. Owens

Filed: June 7, 2001

Title: SEMICONDUCTOR DEVICE

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OCT 07 2003

**OFFICE OF PETITIONS**

Attention: Office of Petitions  
Mail Stop Petition  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

NOTE: If information or assistance is needed in completing this form, please contact Petitions Information at (703)305-9382.

The above-identified application became abandoned for failure to file a timely and proper reply to a notice or action by the United States Patent and Trademark Office. The date of abandonment is the day after the expiration date of the period set for reply in the Office notice or action plus any extensions of time actually obtained.

**APPLICANT HEREBY PETITIONS FOR REVIVAL OF THIS APPLICATION**

NOTE: A grantable petition requires the following items:

- (1) Petition fee;
- (2) Reply and/or issue fee;
- (3) Terminal disclaimer with disclaimer fee -- required for all utility and plant applications filed before June 8, 1995, and for all design applications; and
- (4) Adequate showing of the cause of unavoidable delay

1. Petition fee

Small entity - fee \$ \_\_\_\_\_ (37 CFR 1.17(l)) Applicant claims small entity status..  
See 37 CFR 1.27.

Other than small entity - fee \$ 110.00 (37 CFR 1.17(l)).

2. Reply and/or fee

A. The reply and/or fee to the above-noted Office action in the form of

Amendment and Response to Office Action \_\_\_\_\_ (identify the type of reply):

has been filed previously on August 5, 2002.  
 is enclosed herewith.

B. The issue fee of \$ \_\_\_\_\_

has been paid previously on \_\_\_\_\_.  
 is enclosed herewith.

10/07/2003 AUS DAF1 0000006 09876396

(Page 1 of 3)

01 FDC1452

This collection of information is required by 37 CFR 1.137(a). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED  
UNAVOIDABLY UNDER 37 CFR 1.137(a)**

Docket Number (Optional)

## 3. Terminal disclaimer with disclaimer fee

Since this utility/plant application was filed on or after June 8, 1995, no terminal disclaimer is required.

A terminal disclaimer (and disclaimer fee (37 CFR 1.20(d)) of \$ \_\_\_\_\_ for a small entity of  
\$ \_\_\_\_\_ other than a small entity) disclaiming the required period of time enclosed herewith  
(see PTO/SB/63).

## 4. An adequate showing of the cause of the delay, and that the entire delay in filing the required reply from the due date for the reply until the filing of a grantable petition under 37 CFR 1.137(a) was unavoidable, is enclosed.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorize on PTO-2038.**

October 2, 2003

Date

Signature

516-742-4343

Telephone Number:

Paul J. Esatto, Jr.

Typed or printed name

30,749

Registration Number, if applicable

400 Garden City Plaza

Address

Garden City, NY 11530

Address

Enclosures:  Fee Payment Reply Terminal Disclaimer Form Additional sheets containing statements establishing unavoidable delay Statement with Exhibits A-C

**CERTIFICATE OF MAILING OR TRANSMISSION [37 CFR 1.8(a)]**

I hereby certify that this correspondence is being:

deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: **Mail Stop Petition**, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

transmitted by facsimile on the date shown below to the United States Patent and Trademark Office at (703) 308-6916.

10/2/03

Date

Signature

Paul J. Esatto, Jr.

Typed or printed name of person signing certificate

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

**PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED  
UNAVOIDABLY UNDER 37 CFR 1.137(a)**

NOTE: The following showing of the cause of unavoidable delay must be signed by all applicants or by any other party who is presenting statements concerning the cause of delay.

---

October 2, 2003

Date

  
Signature

---

30,749  
Registration Number, if applicable

---

Paul J. Esatto, Jr.  
Typed or printed name

(In the space provided below, please explain in detail the reasons for the delay in filing a proper reply)

Please see attached STATEMENT FOR PETITION FOR REVIVAL OF AN APPLICATION FOR PATENT ABANDONED UNAVOIDABLY UNDER 37 C.F.R. 1.137(a) WITH EXHIBITS A-C

*(Please attach additional sheets if additional space is necessary)*



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicant(s):** Syuuichi KARIYAZAKI

**Examiner:** Douglas W. Owens

**Serial No:** 09/876,396

**Art Unit:** 2811

**Filed:** June 7, 2001

**Docket:** 14701

**For:** SEMICONDUCTOR DEVICE

**Dated:** October 2, 2003

Assistant Commissioner for Patents  
United States Patent and Trademark Office  
Washington, D.C. 20231

RECEIVED  
OCT 07 2003  
OFFICE OF PETITIONS

**STATEMENT FOR PETITION FOR REVIVAL**  
**OF AN APPLICATION FOR PATENT ABANDONED**  
**UNAVOIDABLY UNDER 37 C.F.R. §1.137(a) (LARGE ENTITY)**

Sir:

In response to the Notice of Abandonment mailed August 20, 2003, and in conjunction with the accompanying Petition for Revival of an Application for Patent Abandoned Unavoidably Under 37 C.F.R. §1.137(a) (Large Entity), the applicant's representative, Paul J. Esatto, Jr. hereby states that the entire delay in filing the required reply from the due date for the required reply until the due date for a grantable petition under 37 C.F.R. §1.137(a) was unavoidable.

**CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on October 2, 2003.

**Dated:** October 2, 2003

  
Paul J. Esatto, Jr.

The applicant's representative received a Notice of Non-Compliant Amendment dated August 14, 2003. In response thereto attorney Eric Halber called Examiner Thomas advising him that the amendment filed on August 5, 2002 was in compliance with the PTO requirements and that a clean version accompanied the marked-up version of the Amendment. A copy of the Amendment as filed together with a postcard receipt is enclosed as Exhibit A. As can be clearly seen, pages 2-6 contain clean version of the amended paragraphs of the specification and pages 6 and 7 contain a clean version of claim 3. The Examiner told Mr. Halber that he would review the case and call back. After reviewing the docket, the Examiner called Mr. Halber back and confirmed that the amendment was in full compliance. Mr. Halber made a handwritten note of these conversations. Please see attached note of Eric Halber, Exhibit B. In view of the phone call back from the Examiner, Mr. Halber understood that the Examiner would withdraw the Notice of Non-Compliance. Mr. Halber prepared an Omission or Correction Memo regarding the Office Action with the notation "\*Mistake on PTO's end. No Action Needed". The note is attached as Exhibit C.

On March 31, 2003 Examiner Owens from the Patent Office called and spoke with Anna Eberle, assistant to Paul J. Esatto, Jr., who again advised the Patent Office of the conversations between Mr. Halber and Examiner Thomas, and further indicated that the response was in compliance. Examiner Owens did not state that the application was abandoned at that time. Ms. Eberle made her own notation of the conversation with Examiner Owens on the Omission or Correction Memo of Mr. Halber, see Exhibit C.

Upon receipt of the Notice of Abandonment dated August 20, 2003, Examiner Tom Thomas was contacted again and he advised that he had no recollection of the telephone conference with Eric Halber regarding the non-compliance and that we would have to file a Petition to Revive.

The applicant's representative is hereby requesting, in conjunction with the accompanying Petition for Revival of an Application for Patent Abandoned Unintentionally Under 37 C.F.R. §1.137(b) (Large Entity), that the Amendment and Response to Office Action which was mailed on August 1, 2002, and sent to the Examiner by first class mail be entered for reconsideration of the application.

Therefore, the applicant's representative requests reinstatement of the application and a waiver of the fee required under 37 C.F.R. 1.137(b).

Respectfully submitted,

  
Paul J. Esatto, Jr.  
Registration No.: 30,749

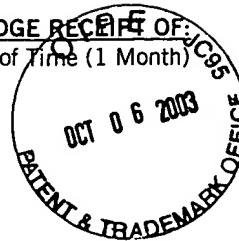
SCULLY, SCOTT, MURPHY & PRESSER  
400 Garden City Plaza  
Garden City, New York 11530  
(516) 742-4343/4366 Fax

PJE:ae  
Encl.

Exhibit A

**PATENT OFFICE DATE STAMP WILL ACKNOWLEDGE RECEIPT OF:**

1. Combined Amendment & Petition for Extension of Time (1 Month)  
Transmittal in duplicate
2. Response
3. Check in the amount of \$110.00
4. Certificate of Mailing dated August 1, 2002



Applicants: Syuuichi KARIYAZAKI

Serial No.: 09/876,396

Filed: June 7, 2001

For: SEMICONDUCTOR DEVICE

Docket: 14701

Dated: August 1, 2002

EPH:ko

**PATENT OFFICE DATE STAMP WILL ACKNOWLEDGE RECEIPT OF:**

1. Combined Amendment & Petition for Extension of Time (1 Month)  
Transmittal in duplicate
2. Response
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4. Certificate of Mailing dated August 1, 2002

Applicants: Syuuichi KARIYAZAKI

Serial No.: 09/876,396

Filed: June 7, 2001

For: SEMICONDUCTOR DEVICE

Docket: 14701

Dated: August 1, 2002

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OCT 07 2003

OFFICE OF PETITIONS

B. ORIGINAL DOCUMENT PRINTED ON CHEMICAL REACTIVE PAPER WITH MICROPRINTED BORDER. SEE REVERSE SIDE FOR COMPLETE SECURITY FEATURES. B.

50-1063/214  
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30451

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C 1109				
M 205				
D 14701				

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PAY

DATE	TO THE ORDER OF	
8/1/03	Commissioner of Patents	

DOLLARS

CHECK AMOUNT

110m

BUSINESS ACCOUNT

THE BANK OF STEWART AVE. & CLINTON ROAD  
GARDEN CITY, N.Y. 11530

Michael J. O'Connor



030451 0214106371 6900648616

THIS DOCUMENT CONTAINS HEAT SENSITIVE INK. TOUCH OR PRESS HERE - RED IMAGE DISAPPEARS WITH HEAT.

**COMBINED AMENDMENT & PETITION FOR EXTENSION OF  
TIME UNDER 37 CFR 1.136(a) (Large Entity)**

Docket No.

In Re Application Of: **Syuuichi KARIYAZAKI**

Serial No.  
09/876,396

Filing Date

Examiner

Group Art Unit  
2811

Invention: **SEMICONDUCTOR DEVICE**

TO THE ASSISTANT COMMISSIONER FOR PATENTS:

This is a combined amendment and petition under the provisions of 37 CFR 1.136(a) to extend the period for filing a response to the Office Action of April 1, 2002 in the above-identified application.  
*Date*

The requested extension is as follows (check time period desired):

One month  Two months  Three months  Four months  Five months

from: July 1, 2002 *Date* until: August 1, 2002 *Date*

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OCT 07 2003

## OFFICE OF PETITIONS

The fee for the amendment and extension of time has been calculated as shown below:

**CLAIMS AS AMENDED**

	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST # PREV. PAID FOR	NUMBER EXTRA CLAIMS PRESENT	RATE	ADDITIONAL FEE
TOTAL CLAIMS	11 -	20 =	0	x \$18.00	\$0.00
INDEP. CLAIMS	1 -	3 =	0	x \$84.00	\$0.00
FEE FOR AMENDMENT					\$0.00
FEE FOR EXTENSION OF TIME					\$110.00
TOTAL FEE FOR AMENDMENT AND EXTENSION OF TIME					\$110.00

COMBINED AMENDMENT & PETITION FOR EXTENSION OF  
TIME UNDER 37 CFR 1.136(a) (Large Entity)

Docket No.  
14701

The fee for the amendment and extension of time is to be paid as follows:

A check in the amount of \$110.00 for the amendment and extension of time is enclosed.

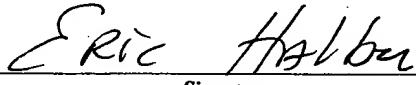
Please charge Deposit Account No. in the amount of \$110.00  
A duplicate copy of this sheet is enclosed.

The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 19-1013/SSMP  
A duplicate copy of this sheet is enclosed.

Any additional filing fees required under 37 C.F.R. 1.16.

Any patent application processing fees under 37 CFR 1.17.

If an additional extension of time is required, please consider this a petition therefor and charge any additional fees which may be required to Deposit Account No. A duplicate copy of this sheet is enclosed.



Signature

Dated: August 1, 2002

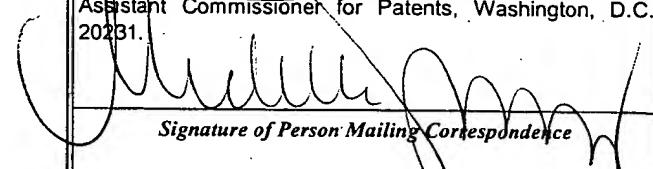
Eric P. Halber  
Registration No.: 46,378

SCULLY, SCOTT, MURPHY & PRESSER  
400 Garden City Plaza  
Garden City, NY 11530  
(516) 742-4343

EPH:ko

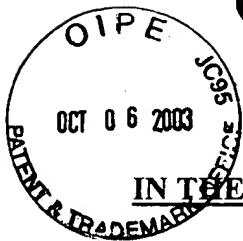
CC:

I certify that this document and fee is being deposited on August 1, 2002 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

  
Signature of Person Mailing Correspondence

Mishelle Mustafa

Typed or Printed Name of Person Mailing Correspondence



PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Applicant(s):** Syuuichi KARIYAZAKI

**Examiner:** Patricia M. Costanzo

**Serial No:** 09/876,396

**Art Unit:** 2811

**Filed:** June 7, 2001

**Docket:** 14701

**For:** SEMICONDUCTOR DEVICE

**Dated:** August 1, 2002

Assistant Commissioner for Patents  
United States Patent and Trademark Office  
Washington, D.C. 20231

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OFFICE OF PETITIONS

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

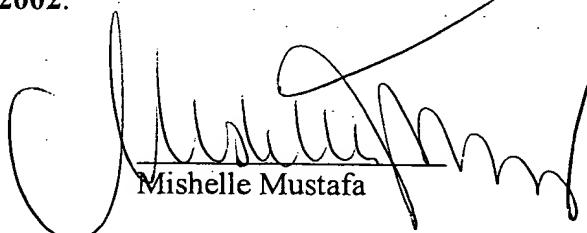
Responsive to the Official Action posted in the above on April 1, 2002, Applicant  
hereby provides the following amendments and remarks for entry of record.

Favorable reconsideration and allowance of the instant case is respectfully requested.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this correspondence is being deposited with the United States  
Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for  
Patents, Washington, D.C. 20231, on **August 1, 2002**.

**Dated:** August 1, 2002

  
Mishelle Mustafa

## IN THE SPECIFICATIONS

Please amend pgs. 11, 12, 14, 16, and 17 as follows:

Pg. 11

The chip 13 is formed by a semiconductor substrate such as silicon, and various elements such as a transistor not shown in the drawing are formed on the bottom main surface of the chip 13 and are covered with a protective dielectric film such as a passivation film. On the surface of the protective dielectric film or on the bottom surface of the chip are formed and arranged ball electrodes 31 made of solder, connected to the above elements, acting as internal electrodes. The ball electrodes 31 are soldered to the interconnect pads 21 formed on the packaging substrate 12 to mount the chip 13 on the packaging substrate 12 in a face-down manner, and the elements in the chip 13 are electrically connected to the ball electrodes 24 on the bottom surface of the packaging substrate 12 through intermediary of the ball electrodes 31 and the interconnect pads 21. The chip 13 is sealed in sealing resin 28.

In the first embodiment, the semiconductor device 11 is mounted on a dielectric substrate, mounting substrate 14. A specified interconnect pattern is formed on the dielectric substrate by using a conductive film to prepare the mounting substrate 14. The interconnect pattern includes interconnect pads 41 connected to the ball electrodes 24 of the semiconductor device 11 and interconnect lines, not shown in the drawings, for connecting the

interconnect pads 41 among one another on the mounting substrate 14 or the interconnect pad 41 with interconnect lines not shown in the drawings for connecting the interconnect pad 41 to an external circuit.

An example of configuration will be described, referring to Fig. 4, in which the ball electrodes 31 are formed and arranged on the bottom surface of the chip 13 of the semiconductor device 11 and interconnect pads 21 are formed and arranged on the top surface of the packaging substrate 12 corresponding to the ball electrodes 31.

The interconnect pads 21 formed on the top surface of the packaging substrate 12 shown in Fig. 5 are disposed corresponding to the ball electrodes 31 on the bottom surface of the chip 13. The ball electrodes 31 on the bottom surface of the chip 13 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in Fig. 5 in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The

22a are connected to each of the interconnect pads 21a of the two outer peripheral I/O cells (CELL-A), and are drawn between the interconnect pads 21a to regions external to the chip 13. On the other hand, the interconnect lines 22b are connected to each of the interconnect pads 21b of the inner peripheral I/O cell (CELL-B), and are drawn similarly to the preceding example in the region of the peripheral I/O cell (CELL-B), and are bundled at a specified interval, at a region out of the inner peripheral I/O cell (CELL-B), to be drawn between the outer peripheral I/O cells (CELL-A) to regions external to the chip 13.

In the structure of the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 12, the density of arranging the interconnect lines 21a at the I/O cells (CELL-A) arranged on the outer periphery of the chip 13 is substantially same as the density of the conventional device shown in Fig.3. However, the density of arranging the interconnect lines 22b connected to the interconnect pad 21b of the I/O cells (CELL-B) arranged inside of the chip 13 can be increased because of the absence of the interconnect pads.

Especially, as shown in Fig.6, since the interconnect lines of the other I/O cells do not pass through the I/O cells (CELL-B) disposed on the inner section of the chip, the I/O cells (CELL-B) may be formed to enable the arrangement of the extremely larger number of the ball electrodes 31 and the interconnect pads 21. An interval may exist between the I/O cells (CELL-B) disposed on the inner section. The ball electrodes 31 and the interconnect pads 21 of the outer peripheral I/O cells (CELL-A) may be freely disposed so long as the spaces through which the interconnect lines 22 of the I/O cells (CELL-B) disposed on the inner section pass may be secured, thereby promoting the higher integration of the semiconductor device having the higher performances. The I/O cells can be freely disposed in the regions of the chip so long as the above requisites are satisfied to increase the freedom of the chip design and the package design.

Since the interconnect pads 21 and the interconnect lines 22 in the embodiment are made by the conductive film having the single layer, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines.

A second embodiment of the present invention is shown in Fig.7 in which the same numerals as those of the first embodiment designate the same elements. A semiconductor device 11 includes a packaging substrate 12A and a chip 13 mounted thereon. The packaging substrate 12A includes a central core layer 211 sandwiched between a pair of buildup layers 212, 213, and a plenty of interconnect pads 21 made of a conductive film are formed on the top buildup layer 212. The interconnect pads 21 are connected to the interconnect lines in each of the multi-layers of the top buildup layer 212, further connected to the bottom buildup layer 213 through intermediary of via plugs, and still further connected to ball electrodes 24 formed on the bottom surface of the bottom buildup layer 213 or the bottom surface of the packaging substrate 12A.

Each of the buildup layers is multi-layered, and the top buildup layer 212 includes five interconnect layers in which a first layer includes the interconnect pads 21 and a ground (GND) layer, a third layer includes a GND layer 3G and a voltage (VDD) layer 3V, and a fifth layer includes a GND layer 5G and a VDD layer 5V connected to the via plugs of the above core layer.

**IN THE CLAIMS:**

**Please amend claim 3 as follows, without prejudice:**

3. (Once amended) The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package for mounting, a semiconductor chip on a packaging substrate, the electrode terminals are ball electrodes disposed on a bottom surface

of said packaging substrate, and the packaging substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon.

**REMARKS**

Applicant thanks the Examiner for acknowledging Applicant's claim to foreign priority, and for confirming that a copy of the Priority Document has been received by the Patent Office. Applicant also thanks the Official Draftsperson for accepting the drawings filed on **June 7, 2001**. As a final matter, Applicant thanks the Examiner for considering the reference submitted with the Information Disclosure Statement dated **July 17, 2001**, as evidenced by the initialed PTO-1449 Form.

The Examiner has objected to the specification under 35 USC § 112, first paragraph, as being unclear. Further, claim 3 stands rejected under 35 USC § 112, second paragraph, as being indefinite. Applicant has amended the specification and claim 3 as shown herein to address the §112 rejections.

Claims 1-11 stand reject under the 35 USC § 103(a) as being unpatentable over U.S. Patent Application Publication, App. No. 09/203196 (Yoon *et, al.*), in view of Lyne (U.S. Patent No. 6,285,560) and Katz (U.S. Patent No. 6,310,398). Because there is no motivation to combine these references, Applicant respectfully traverses the prior art rejection based on the following remarks.

Yoon discloses that lead frame 11 has eight conductors 10a as shown in Fig. 3A such that the number of lead frames can be reduced to one-eighth. On the other hand, Lyne discloses selectively depopulating soldered balls from a solder grid array (BGA) depending on a trace between standard vias, and traces between depopulated vias. Moreover, Katz discloses groups of terminals organized into a plurality of radial spokes extending from the center to the outer perimeter and disposing traces between each of the radial spokes.

According to the present invention, the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The I/O is a single group including a single unit having one or more input-output buffers formed in the chip 13 and an S-terminal (single line terminal), V-terminal (power source terminal) and G-terminal (ground terminal) connected to the input-out-put buffers, or the single I/O cell may include only S-terminals. (Specification pg. 12, line 19- pg. 13, line 4).

In the present invention, a designing method is disclosed for grouping interconnect lines as a single I/O cell (or a block) having a combination of signal/ground/power without dividing the group. The interconnect lines are designed as the same length for the I/O cell and do not cross one another such that connection delays between the lines are reduced and impedance is matched. The density of the interconnect lines is increased by optimizing a space between the I/O cells while maintaining the quality of the signals.

The Examiner admits that Yoon does not explicitly disclose a mounting member including a plurality of electrode terminals electrically and mechanically connected

to respective interconnect pads for mounting a semiconductor chip on a mounting member. Instead, Applicant respectfully submits that the Examiner incorrectly asserts that it would be obvious to modify Yoon's packaging substrate to provide for a mounting member to obtain the advantage of having electrical and mechanical functioning connections to provide for a functioning electrical device.

As shown in Fig. 4 of Yoon, Yoon's package body 20 includes four layers. [0046] Each of Yoon's package layers is heat-adhered to each other by pressure and the via holes are filled with conductive paste T. [0047]. Accordingly, it is clear that Yoon does not disclose, teach or suggest a semiconductor member and a mounting member as recited in independent claim 1.

The semiconductor member of claim 1 includes a plurality of interconnect pads 41. The mounting member (substrate 12) of claim 1 employs a plurality of electrode terminals (internal electrodes 31) which are electrically and mechanically connected to the interconnect pads of the semiconductor member (mounting substrate 14) for mounting the semiconductor chip 13. Of course, Yoon does not disclose, teach or suggest either a semiconductor member or a mounting member, or their recited connections.

In fact, because Yoon's package layers adhere to each other, it would impossible for Yoon, in and of itself, to disclose, teach or suggest the mounting member as recited in independent claim 1. The Examiner does not refer to either Lyne or Katz for the missing mounting member. Accordingly, there is no suggestion or motivation in any of the

applied prior art references to combine theses references (either alone or in combination) in order to meet the claimed limitations of the present invention.

Moreover, even if the applied references were combined, the resulting combination would not produce the claimed limitations of the present invention. Therefore, there would be no reasonable chance of success in obtaining the claimed features of the present invention upon the combination of the applied references. Accordingly, since the Examiner has not met the initial burden of proving a *prima facie* case, the rejection of claims 1-11 under 35 USC § 103 is improper.

Further, since claims 2-11 depend from independent claim 1, these claims are also patentable over the cited references for the same reasons as set out above with respect to independent claim 1. Accordingly, the § 103(a) rejection of claims 1-11 is improper.

Thus, for all the foregoing reasons, all the presently pending claims are believed to be allowable. Since all the presently pending claims are believed to be allowable, and since this application is believed to be otherwise in condition for allowance, Applicant respectfully requests that this application be passed to issue at the earliest possible time.

Respectfully submitted,



Eric P. Halber  
Registration No: 46,378

SCULLY, SCOTT, MURPHY & PRESSER  
400 Garden City Plaza  
Garden City, New York 11530  
516-742-4343  
EPH:ko

**VERSION WITH MARKINGS TO SHOW CHANGES MADE  
IN THE SPECIFICATIONS**

Please amend pgs. 11, 12, 14, 16, and 17 as follows:

Pg. 11

The chip 13 is formed by a semiconductor substrate such as silicon, and various elements such as a transistor not shown in the drawing are formed on the bottom main surface of the chip 13 and are covered with a protective dielectric film such as a passivation film. On the surface of the protective dielectric film or on the bottom surface of the chip are formed and arranged ball electrodes 31 made of solder, connected to the above elements, acting as internal electrodes. The ball electrodes 31 are soldered to the interconnect pads 21 formed on the packaging substrate 12 to mount the chip 13 on the packaging substrate 12 in a face-down manner, and the elements in the chip 13 are electrically connected to the ball electrodes 24 on the bottom surface of the packaging substrate 12 through intermediary of the ball electrodes 31 and the interconnect pads 21. The chip 13 is sealed is sealing resin 28.

In the first embodiment, the semiconductor device 11 is mounted on a dielectric substrate, mounting substrate 14. A specified interconnect pattern is formed on the [a] dielectric substrate by using a conductive film to prepare the mounting substrate 14. The interconnect pattern includes interconnect[s] pads 41 connected to the ball electrodes 24 of the semiconductor device 11 and interconnect lines, not shown in the drawings, for connecting the

interconnect pads 41 among one another on the mounting substrate 14 or the interconnect pad 41 with interconnect lines not shown in the drawings for connecting the interconnect pad 41 to an external circuit.

An example of configuration will be described, referring to Fig. 4 [5], in which the ball electrodes 31 are formed and arranged on the bottom surface of the chip 13 of the semiconductor device 11 and interconnect pads 21 are formed and arranged on the top surface of the packaging substrate 12 corresponding to the ball electrodes 31.

The interconnect pads 21 formed on the top surface of the packaging substrate 12 shown in Fig. 5 are disposed corresponding to the ball electrodes 31 on the bottom surface of the chip 13. The ball electrodes 31 on the bottom surface of the chip 13 are arranged in the shape of a lattice and the interconnect pads 21 are also arranged in the shape of the lattice corresponding to the ball electrodes 31. The specified number of the ball electrodes 31 and the interconnect pads 21 are grouped as a single I/O cell as shown in Fig. 5 in which only the interconnect pads 21 are shown, and these are arranged as the I/O cell unit. In the embodiment, the plenty of the interconnect pads 21 are divided such that the single I/O cell includes an array of 4 x 3 interconnect pads 21. The

22a are connected to each of the interconnect pads 21a of the two outer peripheral I/O cells (CELL-A), and are drawn between the interconnect pads 21a to regions external to the chip 13.

On the other hand, the interconnect lines 22b are connected to each of the interconnect pads 21b of the inner peripheral I/O cell (CELL-B), and are drawn similarly to the preceding example in the region of the peripheral I/O cell (CELL-B), and are bundled at a specified interval, at a region out of the inner peripheral I/O cell (CELL-B), to be drawn between the outer peripheral I/O cells (CELL-A) to regions external to the chip 13.

In the structure of the interconnect pads 21 and the interconnect lines 22 on the packaging substrate 12, the density of arranging the interconnect lines 21a at the I/O cells (CELL-A) arranged on the outer periphery of the chip 13 is substantially same as the density of the conventional device shown in Fig.3. However, the density of arranging the interconnect lines 22b [21b] connected to the interconnect pad 21b of the I/O cells (CELL-B) arranged inside of the chip 13 can be increased because of the absence of the interconnect pads.

Especially, as shown in Fig.6, since the interconnect lines of the other I/O cells do not pass through the I/O cells (CELL-B) disposed on the inner section of the chip, the I/O cells (CELL-B) may be formed [endlessly or annually] to enable the arrangement of the extremely larger number of the ball electrodes 31 and the interconnect pads 21. An interval may exist between the I/O cells (CELL-B) disposed on the inner section. The ball electrodes 31 and the interconnect pads 21 of the outer peripheral I/O cells (CELL-A) may be freely disposed so long as the spaces through which the interconnect lines 22 of the I/O cells (CELL-B) disposed on the inner section pass may be secured, thereby promoting the higher integration of the semiconductor device having the higher performances. The I/O cells can be freely disposed in the regions of the chip so long as the above requisites are satisfied to increase the freedom of the chip design and the package design.

Since the interconnect pads 21 and the interconnect lines 22 in the embodiment are made by the conductive film having the single layer, the interconnect lines connected to the single I/O cell are not crossed in the vertical direction to easily perform the impedance matching on each of the interconnect lines.

A second embodiment of the present invention is shown in Fig. 7 in which the same numerals as those of the first embodiment designate the same elements. A semiconductor device 11 includes a packaging substrate 12A and a chip 13 mounted thereon. The packaging substrate 12A includes a central core layer 211 sandwiched between a pair of buildup layers 212, 213, and a plenty of interconnect pads 21 made of a conductive film are formed on the top buildup layer 212. The interconnect pads 21 are connected to the interconnect lines in each of the multi-layers of the top buildup layer 212, further connected to the bottom buildup layer 213 through intermediary of via plugs, and still further connected to ball electrodes 24 formed on the bottom surface of the bottom buildup layer 213 or the bottom surface of the packaging substrate 12A.

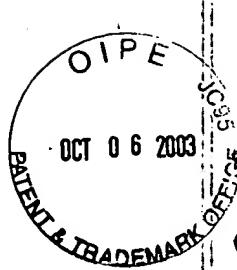
Each of the buildup layers is multi-layered, and the top buildup layer 212 includes five interconnect layers in which a first layer includes the interconnect pads 21 and a ground (GND) layer, a third layer includes a GND layer 3G and a voltage (VDD) layer 3V, and a fifth layer includes a GND layer 5G and a VDD layer 5V connected to the via plugs of the above core layer.

**IN THE CLAIMS:**

**Please amend claim 3 as follows, without prejudice:**

3. (Once amended) The semiconductor device as defined in claim 1, wherein the mounting member is a semiconductor package for mounting, a semiconductor chip on a packaging substrate, the electrode terminals are ball electrodes disposed on a bottom surface of [the] said packaging substrate, and the packaging substrate is a mounting substrate for forming a specified circuit by mounting the semiconductor package thereon.

Exhibit B



9/16/02

14701

Call to Examiner Thomas

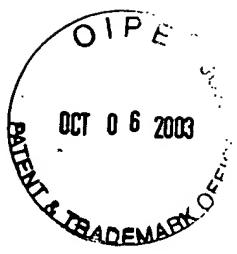
Spoke to Examiner regarding notice of non-compliance for amendment filed on 8/5/02. Informed Examiner that, as filed, the amendment complied with required that a clean version accompany the marked-up version of amendment. Examiner told we he would review case and call me back.

CRIZ Harbor

- After review, Examiner said amendment was in full compliance.

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Exhibit C



## OMISSION OR CORRECTION

C# 1109  
M# 2025  
D# 14701

Due Date: September 14, 2002

(lat.)

Amendment and Response filed August 1, 2002

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\*Mistake on PTO's end.  
No action needed.

Ex. Ows 3B1/03  
TB-308-6167  
called - why no response to  
missin - top reminder, etc.  
Rae